REMARKS

Claims 1-2 and 4-18 are pending. Claims 12-18 have been withdrawn from consideration pursuant to applicants' Response to Restriction Requirement of September 24, 2004. Claim 1 has been amended herein. Support for the amendment is detailed below

Applicants' Response to Claim Rejections under 35 U.S.C. §103

Claims 1-7, 9 and 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (U.S.P. 6,452,274) in view of Matsunaga et al. (U.S.P. 6,559,548) and Hagiwara (JP 2001-168093A). In response thereto, applicants have amended claim 1 to more distinctly claim the subject matter regarded as the invention. Specifically, amended claim 1 states the second dummy pattern comprises a plurality of discrete patterns which are adjacent to each other and disposed at even intervals. Applicants respectfully submit that in light of this amendment, all the limitations of the current invention are not set forth in the cited references.

As described in applicants response of February 28, 2005, the present invention per claim 1 has a feature that the semiconductor device includes the first and the second dummy patterns formed near the interconnection structure, the second dummy pattern is connected to the first dummy pattern through a via portion, and the second dummy pattern includes a plurality of discrete patterns which are adjacent to each other and disposed at even intervals so as to make a pattern density substantially uniform in plane. According to these features of amended claim 1, the first and the second insulating film can be prevented from cracking or peeling due to

mechanical and/or thermal stresses at the interface between the first insulating film and second insulating film or in the first and the second insulating films.

Applicants respectfully submit that the relevant prior art, Hasegawa et al. does not disclose this feature of amended claim 1. Hasegawa et al. discloses in Fig. 7F the semiconductor device including the dummy interconnections 72, 82 formed near the interconnections 71, 81. However, the dummy interconnections 72, 82 of Hasegawa et al. are formed as the paths for heat dispersion. The patterns of the dummy interconnections 72, 82 are closely related to the patterns of the interconnections 71, 81, and are arranged in consideration of the relationship with the patterns of the interconnections 71, 81. Thus, the dummy interconnections 72, 82 of Hasegawa et al. are not disposed at even intervals so as to make a pattern density substantially uniform in plane.

Hagiwara discloses in Fig. 1 the semiconductor device including the dummy interconnections 2, 8 connected to each other via the dummy via-hole 7. However, the dummy interconnections 2, 8 of Hagiwara are formed for preventing the inter-layer insulating films from peeling off or cracking by the thermal stress applied to the outer peripheral part of the semiconductor chip. Thus, the dummy interconnections 2, 8 of Hagiwara are not disposed at even intervals so as to make a pattern density substantially uniform in plane.

Matsunaga et al. discloses the interconnection buried in the insulating film. However, Matsunaga et al. neither teaches nor suggests the dummy interconnection pattern formed near the interconnection.

As described above, Hasegawa et al. and Hagiwara clearly differ from the present invention and do not provide any motivation for the present invention. Matsunaga et al. neither teaches nor suggests the dummy interconnection pattern. Thus, applicants respectfully submit that in light of the amendment to claim 1, claims 1-7, 9 and 10 would not have been obvious to one of ordinary skill in the art at the time the invention was made. The combination of Hasegawa et al., Hagiwara and Matsunaga et al. does not disclose all the limitations of the currently claimed invention.

Applicants respectfully address the remarks of the Office Action as follows. The Office Action states that "Applicant contends that the dummy patterns of Hasegawa et al. differ from those of the invention since they are provided for the heat dispersion and not for reducing intra-plane variations of a polishing amount in the CMP process. However, the limitations as recited in claims 1-11 do not include such features."

As described above, the dummy interconnections 72, 82 of Hasegawa et al. are formed as the paths for heat dispersion, and are not disposed at even intervals so as to make a pattern density substantially uniform in plane. Applicants respectfully submit that it is apparent from the limitations of claims 1-11 that the dummy patterns of the present invention clearly differ from the dummy interconnections 72, 82 of Hasegawa et al.

It is apparent from the specification of the present application that the dummy pattern including a plurality of discrete patterns, which are adjacent to each other and disposed at even intervals formed so as to make a pattern density substantially uniform in plane, means the

dummy pattern for reducing intra-plane variations of a polishing amount in the CMP process (see, e.g., page 14, lines 8-18 of the specification). Thus, the teaching of the specification is the basis for the limitations as recited in claims 1-11.

The Office Action also states that "Applicant contends that the dummy patterns of Hagiwara are formed only in the peripheral regions and not in the whole region/major part of the chip. However, the limitations as recited in claims 1-11 include the dummy patterns being near to interconnection structure, but do not include those being in the major part of the chip."

Applicants submit that it is apparent from the limitations as recited in claims 1-11 that the dummy patterns of the present invention are formed in the whole semiconductor chip. Specifically, in light of the specification of the present application the limitation: "so as to make a pattern density of the second conducting layer substantially uniform in plane" as recited in claim 1 means that the dummy patterns are formed in the whole semiconductor chip region (see, e.g., page 14, lines 13-17 of the specification). Thus, applicants' arguments are based on the limitations as recited in claims 1-11.

Claim 11 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hasegawa et al. in view of Matsunaga et al. Wherefore, for the reasons set forth above, applicants respectfully submit that claim 11 is not obvious over Hasegawa et al. in view of Matsunaga et al.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al., Matsunaga et al. and Hagiwara in view of Shaffer, II et al. (U.S. 2002/0052125A). As described above, Hasegawa et al. and Hagiwara clearly differs from the present invention of amended claim 1 on which claim 8 depends. Therefore, in light of the remarks above as to claim 1 applicants

respectfully submit that claim 8 is addressed by nature of its dependency. In regard to the additionally cited references in the rejection of claim 8, Matsunaga et al. and Shaffer, II et al. neither teach nor suggest the dummy interconnection pattern.

Thus, applicants respectfully submit that claim 8 would have been unobvious to one of ordinary skill in the art at the time of the invention was made, even though Hasegawa et al., Hagiwara, Matsunaga et al. and Shaffer, II et al. are combined.

For at least the foregoing reasons, it is believed that this application is now in condition for allowance. If, for any reason, it is believed that this application is not in condition for allowance, Examiner is encouraged to contact the Applicants' undersigned attorney at the telephone number below to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

Michael J. Caridi
Attorney for Applicants
Registration No.: 56,171
Telephone: (202) 822-1100
Facsimile: (202) 822-1111

MJC/meu